Abstract of the Disclosure:

An integrated memory includes command terminals for receiving command signals in a normal operation and in a test operation of the memory, and also a signal terminal for receiving a further signal, which differs from the command signals. Registers store data patterns or data topologies for use in the test operation of the memory. A register decoder circuit serves for the selection of the registers, it being possible for inputs of the register decoder circuit to be connected to the command terminals and to the signal terminal for the purpose of selection of the registers in the test operation. The invention makes it possible, for the test operation, to address an increased number of registers without driving an additional external terminal pin. A method for testing the memory is also provided.

GLM/nt